17.9 A High-Conversion-Ratio and 97.4% Peak-Efficiency 3-Switch Boost Converter with Duty-Dependent Charge Topology for 1.2A High Driving Current and 20% Reduction of Inductor DC Current in MiniLED Applications

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Today's miniLED displays can be divided into multiple arrays. Each miniLED array with 900 pixels can have 60 channels where each channel has 15 LEDs connected in series. To drive multi-channel miniLEDs in parallel from a low input voltage V_{IN} (= 6V), a boost converter with high output voltage (up to 30V) and high output current (up to 1.2A for 2000 nits) is required where the conversion ratio (CR=V_{OUT}/V_{IN}) is 5. Since the inductor current $I_L = I_{LOAD} / (1-D)$ of the conventional 2-switch (2S) boost converter is high, where I_{LOAD} is the load current and D is the duty cycle, 2S boost converters have low efficiency and high output voltage ripple. Although the boost converter assisted by a series flying capacitor C_F can reduce the inductor current level to improve efficiency [1-5], C_F lacks energy under high CR and high loading conditions. At the top of Fig. 17.9.1, both techniques in [1] and [2] charge the C_F during φ2. In case of high CR, the duration of φ2 becomes small to seriously affect the charging time. Hence, due to insufficient charge stored in C_F, the driving capability will decrease. At no load (left of Fig. 17.9.2), [1] fails to regulate and D is 0.87 in [2] to have CR=5. Interestingly, both [1] and [2] fail to have CR=5 at load current=1.2A. Although additional dual channel-interleaved three-level buck-boost (DTLBB) structure in [1] can alternatively charge two flying capacitors, the hardware overhead is double and the quiescent current becomes high.

Therefore, to reduce the number of switches as compared to the state-of-the-art designs, a 3-switch (3S) boost converter in this paper is proposed to charge the C_F during φ1 to fit high CR conditions in the bottom of Fig. 17.9.1. At high CR, the extension of φ1 can ensure sufficient charge stored in C_F to increase driving capability at heavy loads. Meanwhile, due to the series connection of the inductor and the C_F during φ2, the inductor current can be lowered by the reduced voltage across the inductor. The maximum voltage stress across the switch is V_{OUT}-V_{IN} (=24V) compared to 2V_{OUT}-V_{IN} (=54V) in [2] and V_{OUT} (=30V) in [4]. In [2], since the series connection contains the inductor, C_F, and C_{OUT}, the insufficient energy stored in C_F under heavy load becomes more serious. On the contrary, during φ1, the proposed 3S boost converter uses V_{IN} to charge the inductor and C_F simultaneously to ensure high driving capability. Thus, the CR of the proposed 3S boost converter can be much higher than that of [2]. On the left side of Fig. 17.9.2, D (duration of φ1) is only 0.73 at CR=5 and no load while the duty increases to 0.81 at load current = 1.2 A. Furthermore, the discontinuous conduction mode (DCM) can be easily realized in 3S boost converter after adding an additional DCM phase φ_{DCM}. The DCM operation in [4] will induce a reverse resonance between the inductor and the capacitor. The φ_{DCM} in the proposed 3S boost converter can significantly increase the light load efficiency since the off-time period is inversely proportional to loading current. More importantly, since only three power switches are used, both switching and conduction losses can be reduced as compared to [1-5].

With the same positive slope (=V_{IN}/L) of I_L, the insertion of C_F can lower the negative slope of I_L to '(2V_{IN}-V_{OUT})/L' compared to large negative slope of '(V_{IN}-V_{OUT})/L' in the 2S boost converter in the bottom right of Fig. 17.9.2. In the continuous current mode (CCM), the proposed 3S boost converter can have a lower inductor AC current ripple I_{L_AC} which is 25% smaller than that of 2S boost converter at CR=5 since $I_{L\_AC(3S)} = [(2D_{(2S)}-1)/ D^2_{(2S)}] \times I_{L\_AC(2S)}$. The 3S boost converter can charge inductor DC current I_{L_DC} by 680mA/cycle (under maximum duty), while the 2S boost converter can only charge I_{L_DC} by 270mA/cycle, thus, fast transient response can be readily guaranteed. Besides, the 3S boost converter has a high CR = (2-D)/(1-D), so only D = 75% is needed to boost V_{OUT} to 5V_{IN}. In contrast, the 2S boost converter requires D = 80%, and [2] requires D = 88%. Unfortunately, [1] and [3] cannot reach 5V_{IN}. Under the same load conditions, a lower φ1 indicates a lower I_{L_DC}. When CR = 5, the I_{L_DC} of the 3S boost converter is 20% smaller than that of the 2S boost converter.

The control loop adopts the hysteresis current mode in Fig. 17.9.3. The hysteresis window 'V_{HYS}' will be optimized by the frequency-controlled right-half-plane (RHP) zero and reduced droop (FRZ-RD) circuit in Fig. 17.9.4. The inductor AC current I_{AC_SIG} generated by the RC network can greatly improve the load regulation since the error caused by inductor DC level can be eliminated by turning on 'S_{RESET}' at the beginning of each cycle [6]. To improve light-load efficiency, a high-precision zero-current-detection (ZCD) circuit is proposed to solve the inaccuracy problem in conventional ZCD circuits. Conventional ZCD circuits in [1-2] will generate larger negative inductor current and power loss due to the lower value of '$I_L \times R_{ON}$' since R_{ON} of the power MOSFET (upper right in Fig. 17.9.3) is small. Due to inherent delay in the comparator, the increasing power loss will significantly reduce the efficiency. Thus, the proposed ZCD uses the C_F to detect the inductor zero current in advance. The bottom left of Fig. 17.9.3 shows the operation of C_F voltage based ZCD pre-detector. In φ2, as the voltage across C_{OUT} increases, I_{COUT} will become lower. When I_{COUT} is equal to zero before φ1, it means that C_{OUT} reaches saturation earlier, and the reverse inductor current will appear later. At the time that $dV_{COUT}/dt = 0$ and $dV_{CF}/dt = dV_Y/dt$, I_{COUT} becomes negative and flows into C_F to cause the decrease of V_X. The generated ZCD_{PRE} signal can indicate whether ZCD occurs by sensing the $dV_X/dt=0$. Finally, the delay ZCD_{PRE} generated by the ZCD least significant bit (LSB) tuner will trigger the ZCD signal to turn off 'S3'.

The frequency-dependent RHP zero of 3S boost converter is higher than that of 2S boost converter (top of Fig. 17.9.4). Thus, changing f_{SW} during transients can reduce the voltage drop when f_{SW} = 0.4MHz (RHP zero at point b =1.93MHz). Recovery time can be reduced when f_{SW} = 2.3MHz (RHP zero at point c = 0.49MHz) [7]. The proposed FRZ-RD circuit can change the hysteresis window "V_{HYS}" corresponding to the load (bottom of Fig. 17.9.4). The detection of error amplifier output V_{EA_LB} can decide whether the transient occurs. In case of light-to-heavy load change, the transient signal V_{TRAN} becomes high and the V_{HYS} is expanded to decrease f_{SW} to work in the droop reduce (DR) mode in Block1. The delayed signal V_{EA_DELAY} compares with V_{EA_LB} to detect whether V_{OUT} starts to rebound in Block2. When V_{HYS} is greatly reduced to enter the short recovery (SR) mode, lower V_{HYS} can increase f_{SW} by moving RHP zero to a lower frequency to achieve fast transients. Finally, the system will return to the steady-state (SS) mode and the RHP zero will return to point a and V_{EA_LB} becomes lower than V_{REF2}. The duration of the restoration signal $V_{RESTORE}$ will make V_{HYS} smoother because the nonlinear effect needs more time to stabilize it.

The test chip is fabricated in a 0.25μm process. The input voltage ranges from 4 to 12V, and the output voltage is regulated to 30V. As shown in Fig. 17.9.5, the proposed 3S boost converter can operate in CCM or DCM to suit the load requirements. The difference between ZCD_{PRE} and ZCD is 58ns (bottom right in Fig. 17.9.5) and can respond to the ZCD detection. The transient response (bottom left of Fig. 17.9.5) shows that the recovery time is 42μs when the load changes from 120mA to 1.2A. Using FRZ-RD technique, the proposed 3S boost converter only needs 8 switching cycles to stabilize I_L but 2S boost converter needs 39 cycles.

The table in Fig. 17.9.6 summarizes the performance of the proposed 3S boost converter and compares it with the state-of-the-art designs. As shown in the table, the proposed design can have the peak efficiency of 97.4%, 95.2%, 91.7% for CR = 2.5, 5, and 7.5, respectively. The chip micrograph is shown in Fig. 17.9.7.

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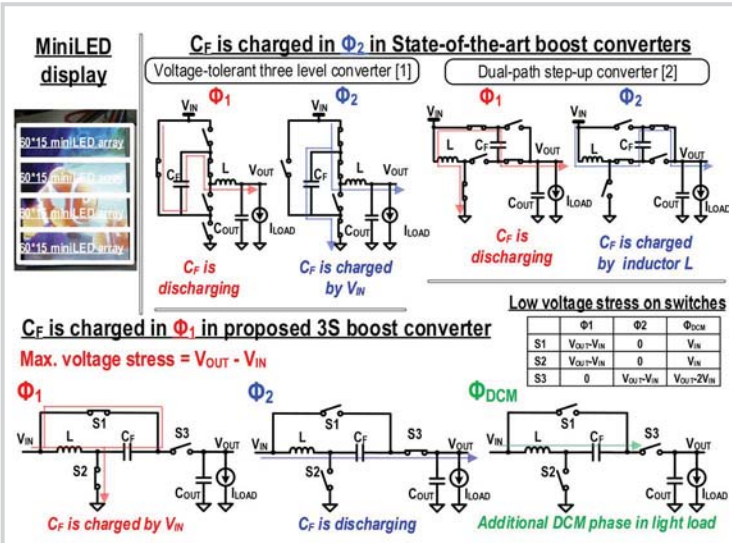


Figure 17.9.1: C_F charged in φ2 in prior arts limits the driving capability in high CR (top); 3S boost converter charges the C_F in φ1 fitting the demand of high CR, high driving capability (bottom) and low voltage stress on switches.

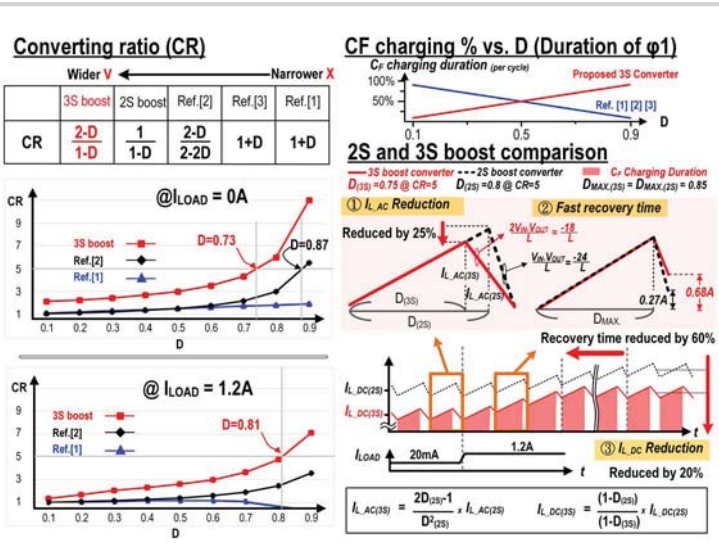


Figure 17.9.2: Proposed 3S boost converter has widest CR either under no load or heavy load. The C_F with sufficient energy can bring low inductor ripple, fast transient response, and low inductor dc current.

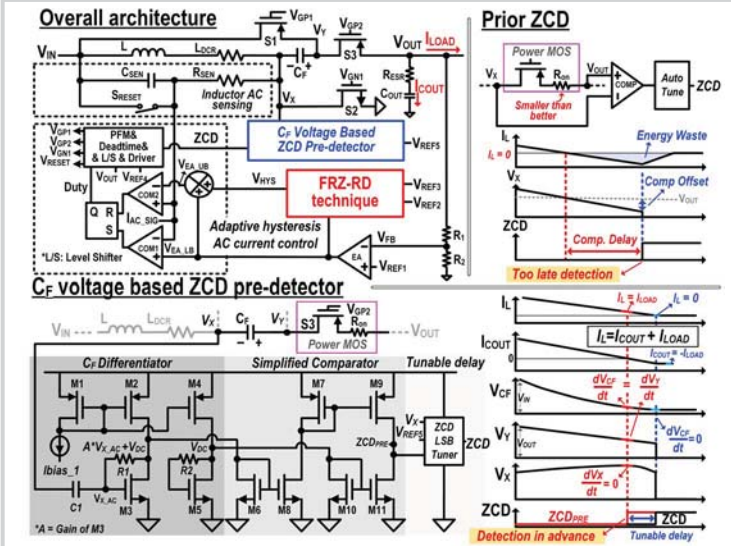


Figure 17.9.3: The overall architecture of the proposed 3S boost converter and the C_F voltage based ZCD pre-detector which can detect the reverse inductor current in advance.

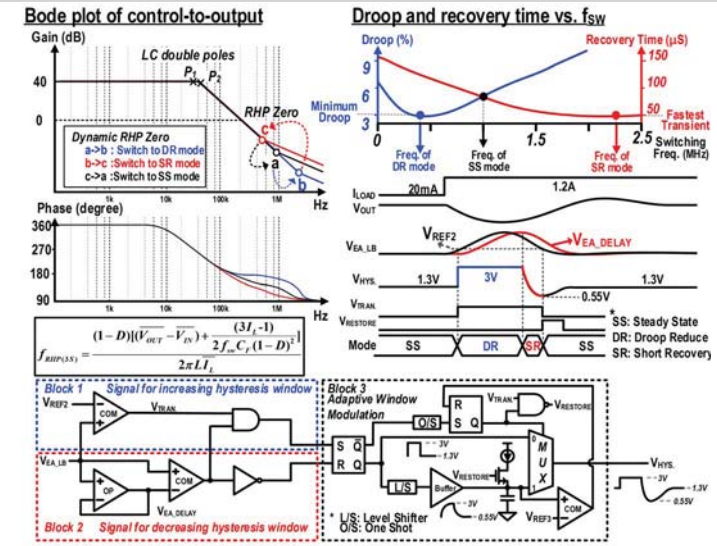


Figure 17.9.4: FRZ-RD circuit can automatically optimize the voltage droop and transient response by adjusting to change the width of the hysteresis window V_{HYS} to change the position of RHP zero.

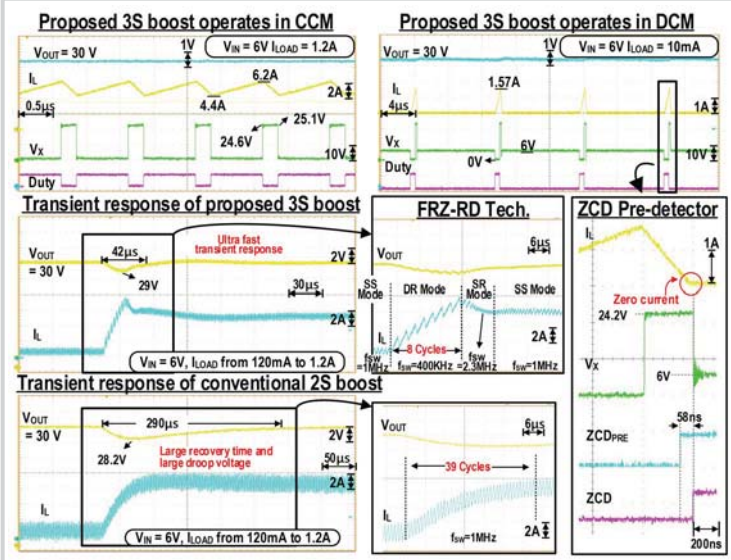
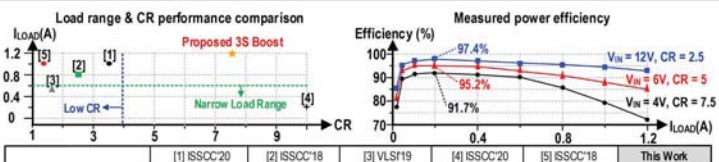


Figure 17.9.5: Measured waveforms of proposed 3S boost converter and conventional 2S boost converter.



	[1] ISSCC'20	[2] ISSCC'18	[3] VLSI'19	[4] ISSCC'20	[5] ISSCC'18	This Work
Process	90nm	0.18μm BCD	0.25μm	0.35μm BCD	0.18μm BCD	0.25μm BCD
Operating mode	buck/boost	boost	buck/boost	boost	buck/boost	3S-boost
Control scheme	#Current mode	Current mode	Time-based Current mode	Voltage mode	Hysteresis Control	Adaptive Hysteresis Control
Input voltage(V)	2.5-5	2-4.2	2.9-6.3	2-4.4	2.7-4.2	6
Output voltage(V)	0.4-9	3-5	4.6	9-20	3.4	30
Inductor & Output Capacitor (C_F)	2.2μH & 4.7μF(10μF*)	4.7μH & 10μF(10μF*)	4.7μH & 10μF(470nF*)	2x3.3μH & 10μF(2x470nF*)	2.2μH & 10μF(2*20μF*)	4.7μH & 4.7μF(2.2uF*)
Load current(mA)	0-1000	10-800	50-600	10-250	30-1000	1-1200
Conversion Ratio @ Boost	1+D	$\frac{2\text{-}D}{2\text{-}2D}$	1+D	$\frac{2}{1\text{-}D}$	$\frac{3\text{-}D}{2}$	$\frac{2\text{-}D}{1\text{-}D}$
Switching frequency(MHz)	0.8-3	1	1.45	2	1	0.4-2.3
Number of switch	5	5	4	6	7	3
DCM (ZCD)	YES (By Mos)	YES (By Mos)	NO	NO	NO	YES (By Cap)
Charging Phase Of Capacitor	φ2	φ2 (By Inductor)	φ2	interleave	φ2	φ1 (By V_{IN})
C_F Charging Duration When Duty Increase	Decrease	Decrease	Decrease	Decrease	Decrease	Increase
Maximum Voltage Stress	V_{IN}	$2V_{OUT}$-V_{IN}	$2V_{IN}$	V_{OUT}	V_{IN}	V_{OUT}-V_{IN}
Max Efficiency @ Boost	96.8%	95.2%	92.75%	93.5%	97.0%	97.4%
Transient Response FOM	NA	11.06	16.63	NA	32.18	38.96

Flying cap #Table paper is not stated, inferred from the graph Transient Response FOM = [CRΔI_{LOAD} (mA)] / [Recovery Time (us)*V_{OUT_Droop} (%)]

Figure 17.9.6: Comparison with the state-of-the-art designs including I_{LOAD} vs. CR, measured efficiency vs. I_{LOAD}, and comparison table.

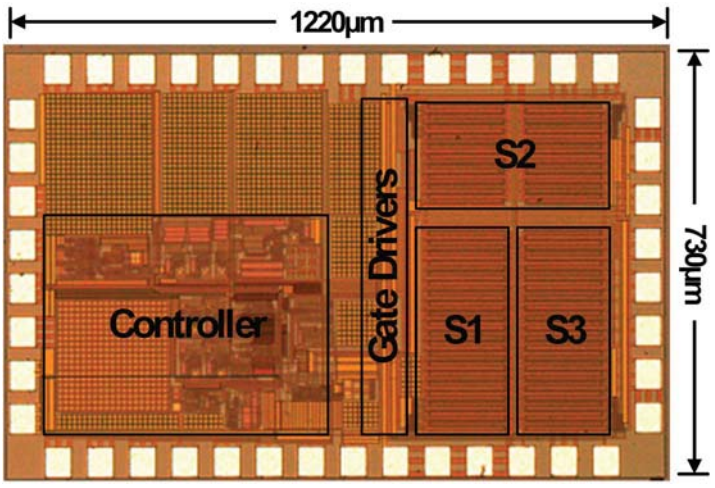


Figure 17.9.7: Die micrograph.

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